WHAT IS CLAIMED IS:

1. A semiconductor fabrication process, comprising:

forming a silicon fin overlying a substrate, the fin having first and second primary faces substantially perpendicular to a surface of the substrate;

forming a gate dielectric on the first and second primary faces of the silicon fin;

forming a gate electrode overlying the gate dielectric; and

forming dielectric spacers confined to regions adjacent to sidewalls of the gate electrode, wherein portions of the primary fin faces outside regions of the dielectric spacers are exposed.

2. The method of claim 1, further comprising forming additional conductive regions overlying the exposed portions of the primary fin faces by epitaxial growth.

3. The method of claim 2, further comprising forming a silicide on the additional conductive regions overlying the exposed portions of the primary fin faces.

4. The method of claim 1, wherein the formation of the gate electrode defines confinement regions adjacent sidewalls of a portion of the gate electrode.

5. The method of claim 4, wherein forming the gate electrode comprises;

depositing a first material over the fin and substrate;

depositing a capping layer over the first material wherein at least one etchant is selective between the capping layer and the first material;

patterning a photoresist overlying the capping layer;

etching through the capping layer and the first material as a function of the patterned photoresist, wherein the etching produces a first material width that is less than a width of the capping layer to further define the confinement regions under the capping layer adjacent sidewalls of the first material.

6. The method of claim 5, wherein the capping layer is a material selected from the group of materials consisting of metal, polysilicon, oxide, and nitride.

7. The method of claim 6, wherein the first material is selected from the group of material comprising polysilicon and silicon germanium.

8. The method of claim 5, further comprising non-selectively depositing a dielectric spacer material and subsequently etching the spacer material to remove the dielectric spacer material everywhere except where the spacer material has filled the confinement regions adjacent the polysilicon sidewalls.

9. The method of claim 5, further comprising performing a spacer etch of the first material prior to depositing the capping layer.

10. The method of claim 1, wherein forming the silicon fin comprises:

depositing a capping dielectric material overlying silicon;

patterning photoresist overlying the capping dielectric to expose portions of the dielectric material; and

etching the exposed portions of the capping dielectric and the underlying silicon to form the fin, wherein the etching includes undercutting the silicon relative to

the capping dielectric wherein the silicon fin has a thinner profile than the capping dielectric.

11. A semiconductor fabrication process, comprising:

forming a silicon fin overlying a substrate, wherein the silicon fin includes first and second primary faces substantially perpendicular to an upper surface of the underlying substrate;

forming a gate dielectric layer on primary faces of the silicon fin;

forming a gate electrode in contact with the gate dielectric layer, wherein the gate electrode leaves portions of the primary faces of the silicon fin exposed;

forming dielectric spacers selectively adjacent sidewalls of the gate electrode wherein portions of the primary fin faces of the dielectric spacers remain exposed after dielectric spacer formation; and

processing the exposed portions of the primary fin faces to reduce their resistivity.

12. The method of claim 11, wherein processing the exposed portions of the primary fin faces includes epitaxially growing silicon on the exposed portions of the primary fin faces.

13. The method of claim 11, wherein processing the exposed portions of the primary fin faces includes forming a silicide on the exposed portions of the primary fin faces.

14. The method of claim 13, wherein forming the gate electrode comprises;

depositing a first material over the fin and substrate;

depositing a capping layer over the first material wherein at least one etchant is selective between the capping layer and the first material;

patterning a photoresist overlying the capping layer;

etching through the capping layer and the first material as a function of the patterned photoresist, wherein the etching produces a first material width that is less than a width of the capping layer to further define the confinement regions under the capping layer adjacent sidewalls of the first material.

15. The method of claim 14, wherein the capping layer is a material selected from the group of materials consisting of metal, polysilicon, oxide, and nitride.

16. The method of claim 15, wherein the first material is selected from the group of material comprising polysilicon and silicon germanium.

17. A transistor within an integrated circuit, comprising:

a silicon fin overlying a substrate, wherein the silicon fin includes first and second primary faces substantially perpendicular to a surface of the underlying substrate;

a gate dielectric on at least portions of the first and second primary faces of the silicon fin;

a gate electrode overlying the gate dielectric, wherein the gate electrode defines channel regions of the transistor within the silicon fin underlying the gate electrode and source/drain regions within remaining portions of the silicon fin; and

dielectric spacers adjacent sidewalls of the gate electrode and confined to the proximity of the gate electrode.

18. The transistor of claim 17, wherein the gate electrode comprises a first material and a capping layer overlying the first material, wherein a width of the first material is less than a width of the capping layer, wherein the dielectric spacers occupy regions under the portion of the capping layer overhanging the first material.

19. The transistor of claim 17, wherein the first material is silicon and the capping layer is material selected from a group of materials consisting of metal, oxide, and nitride.

20. The transistor of claim 17, further comprising, additional conductive material formed on portions of the silicon fin not covered by the gate electrode, wherein the confined spacers prevent electrical conduction between the additional conductive material and the gate electrode.

21. A semiconductor fabrication process, comprising:

forming a silicon fin overlying a substrate, the fin having first and second primary faces substantially perpendicular to a surface of the substrate;

forming a gate dielectric on the first and second primary faces of the silicon fin;

forming a gate electrode overlying the gate dielectric;

forming a capping layer overlying the gate electrode and patterning the capping layer, wherein the capping layer forms a cap overlying the gate electrode and having a lateral dimension greater than a lateral dimension of the underlying gate electrode, further forming a confined region adjacent sidewalls of the gate electrodes; and

forming dielectric spacers confined within the confinement regions adjacent sidewalls of the gate electrode, wherein portions of the primary fin faces outside regions of the dielectric spacers are exposed.